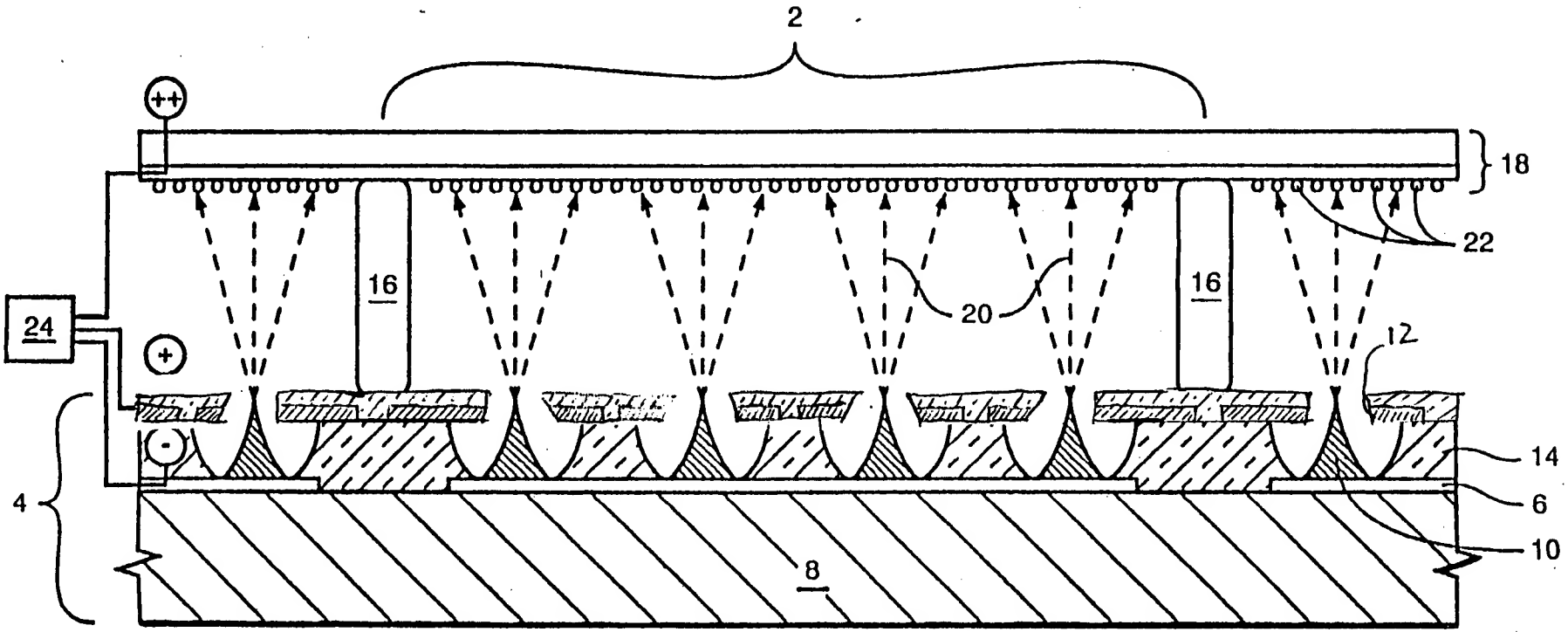
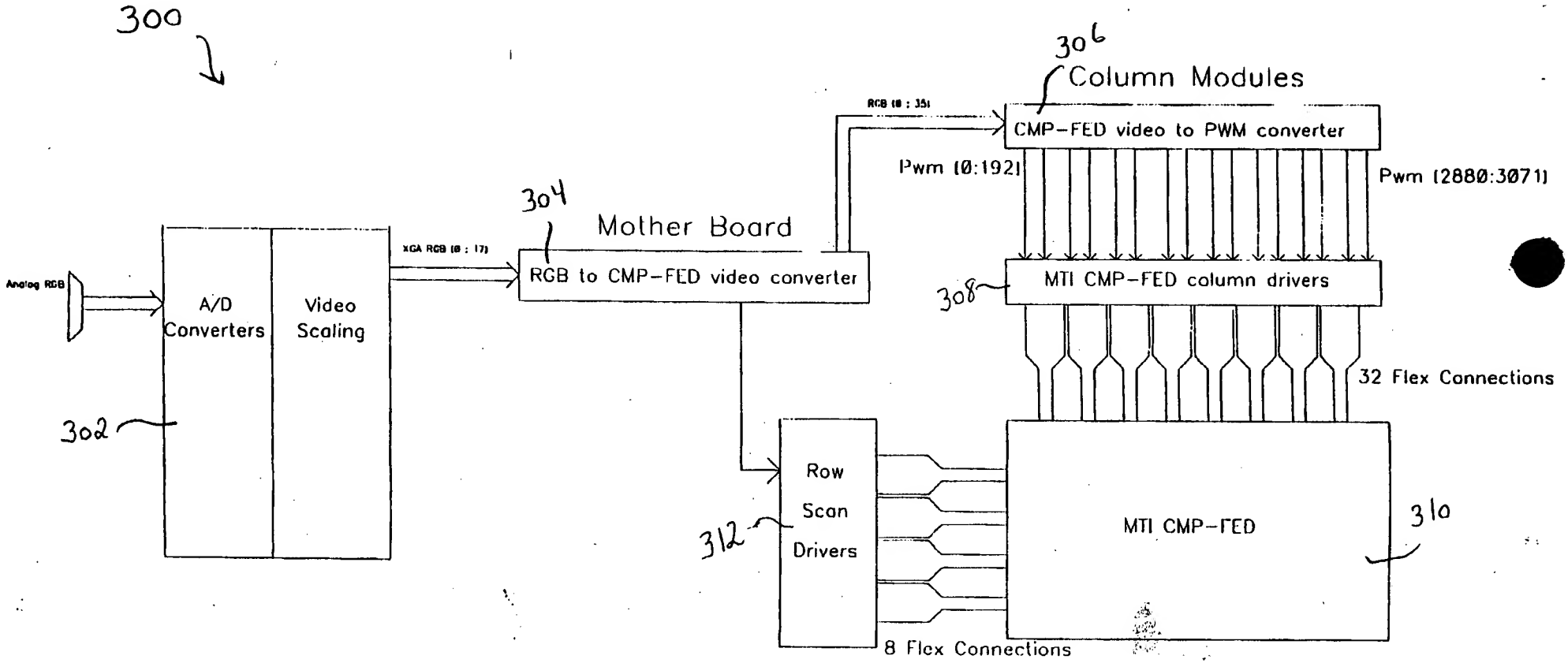


FIG.1

Figure 2


300
306
Column Modules
RGB (0 : 35)
CMP-FED video to PWM converter
Pwm (0:192)
Pwm (2880:3071)
304
Mother Board
XGA RGB (0 : 17)
RGB to CMP-FED video converter
MTI CMP-FED column drivers
308
Analog RGB
A/D Converters
Video Scaling
302
32 Flex Connections
Row Scan Drivers
312
MTI CMP-FED
310
8 Flex Connections

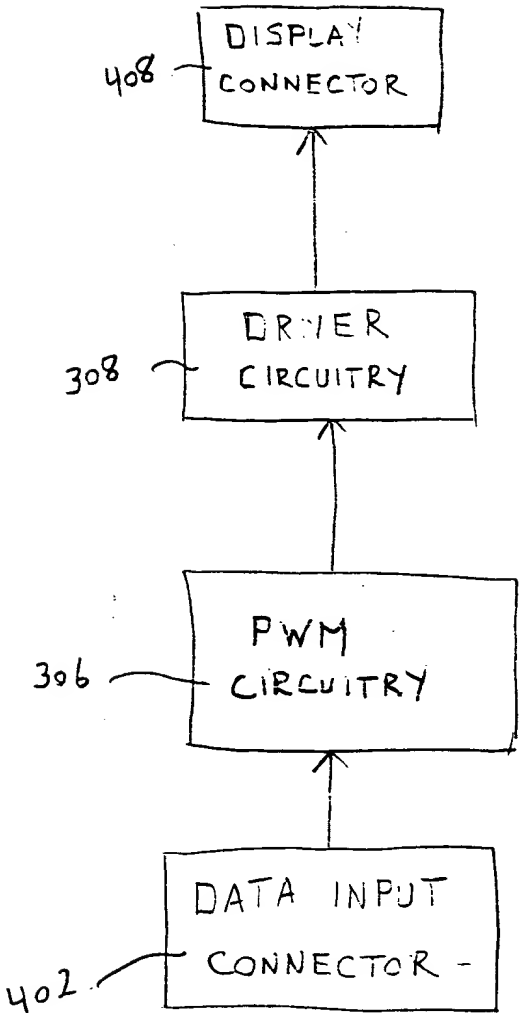

DISPLAY CONNECTOR
408
DRIVER CIRCUITRY
308
PWM CIRCUITRY
306
DATA INPUT CONNECTOR
402
400

Figure 3

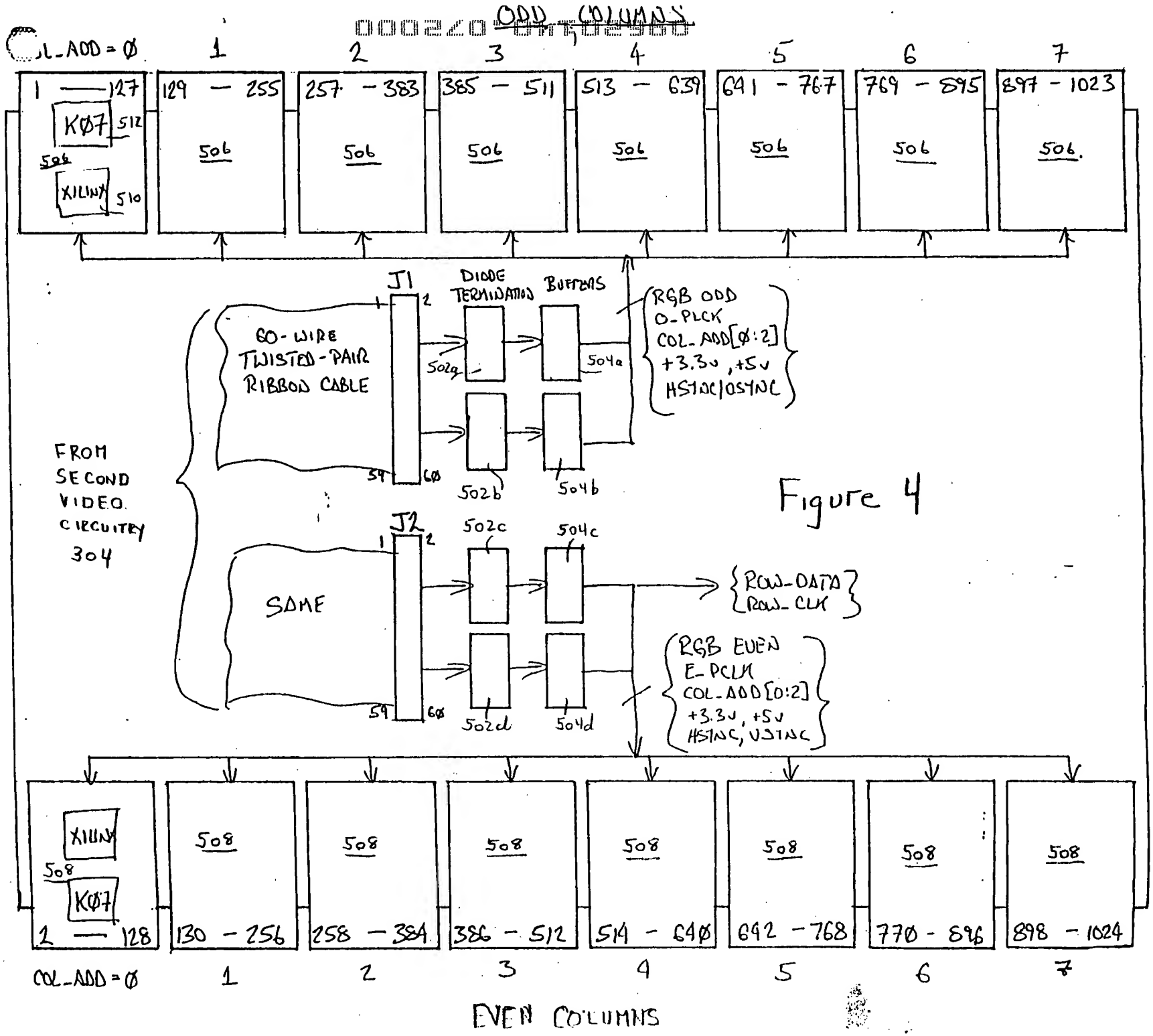

ODD COLUMNS
COL_ADD = Ø
1
2
3
4
5
6
7
1 — 127
129 — 255
257 — 383
385 — 511
513 — 639
641 — 767
769 — 895
897 — 1023
KØ7
512
506
XILINX
510
J1
DIODE TERMINATION
BUFFERS
60-WIRE TWISTED-PAIR RIBBON CABLE
502a
504a
RGB ODD
O-PCLK
COL_ADD[Ø:2]
+3.3V, +5V
HSYNC/VSYNC
FROM SECOND VIDEO CIRCUITRY 304
59
60
502b
504b
J2
502c
504c
SAME
ROW_DATA
ROW_CLK
RGB EVEN
E-PCLK
COL_ADD[0:2]
+3.3V, +5V
HSYNC, VSYNC
502d
504d
508
1 — 128
130 — 256
258 — 384
386 — 512
514 — 640
642 — 768
770 — 896
898 — 1024
COL_ADD = Ø
EVEN COLUMNS

Figure 4

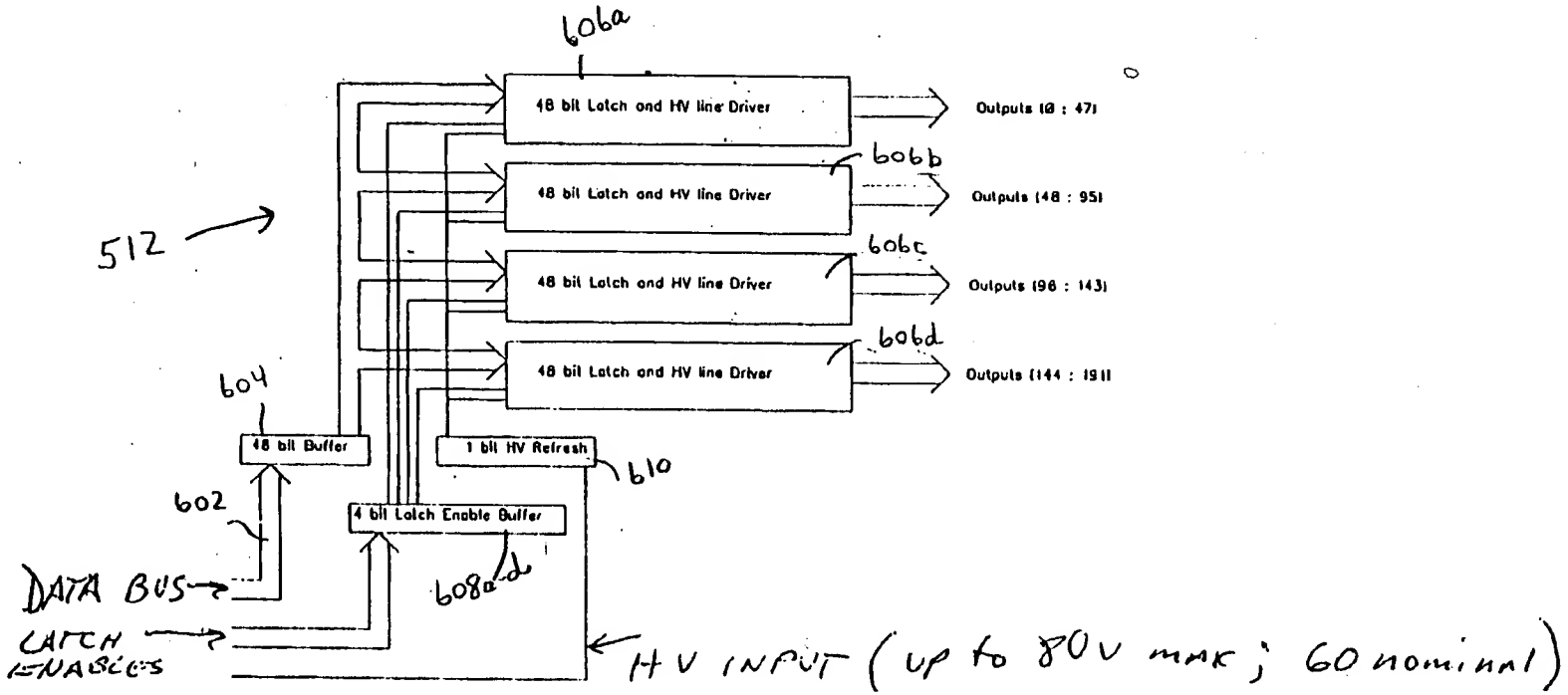

606a
48 bit Latch and HV line Driver
Outputs (0 : 47)
606b
48 bit Latch and HV line Driver
Outputs (48 : 95)
606c
48 bit Latch and HV line Driver
Outputs (96 : 143)
606d
48 bit Latch and HV line Driver
Outputs (144 : 191)
512
604
48 bit Buffer
1 bit HV Refresh
610
602
4 bit Latch Enable Buffer
608a-d
DATA BUS
LATCH ENABLES
HV INPUT (up to 80V max; 60 nominal)

Figure 5

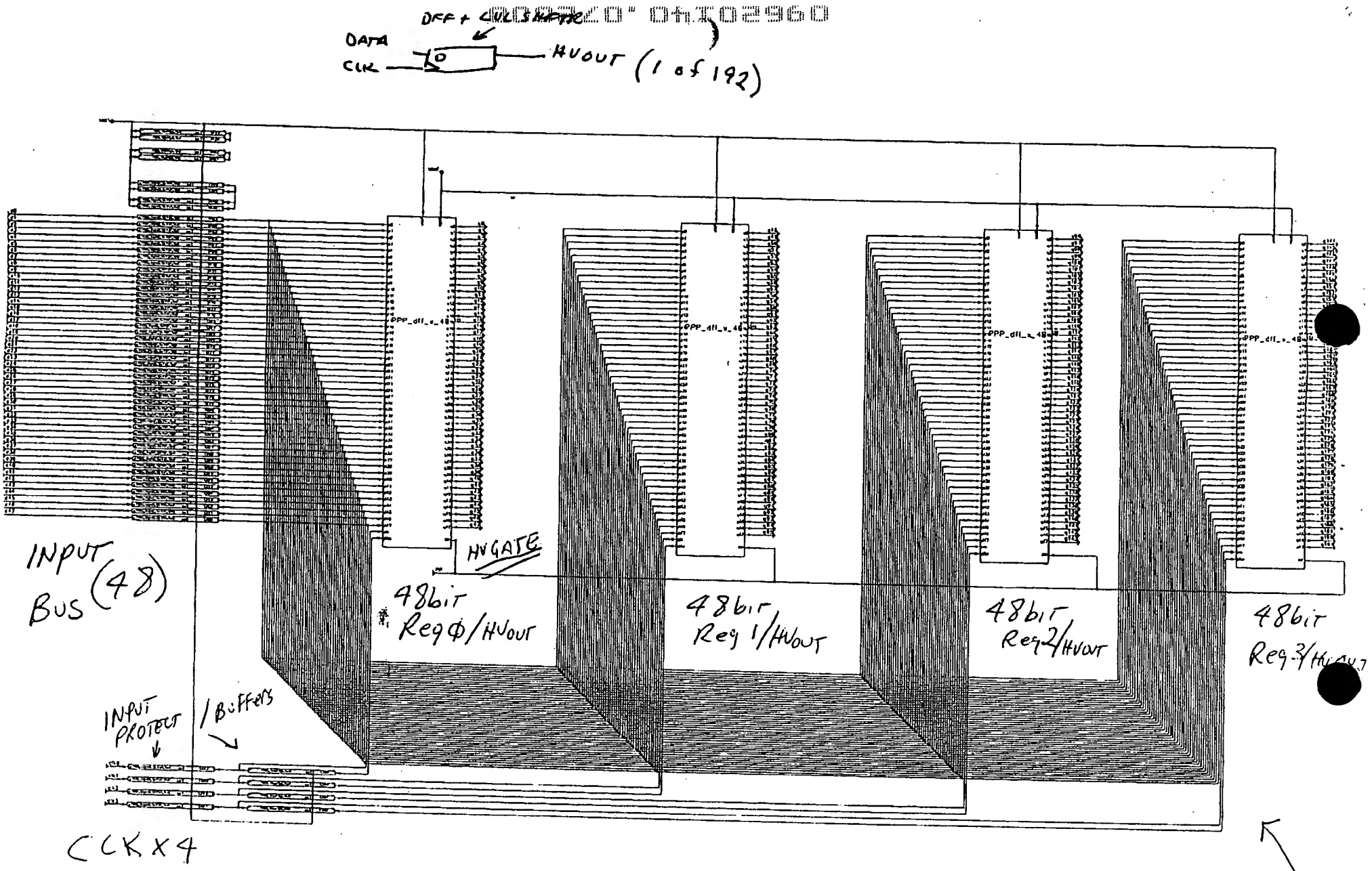

DFF + CURRENT SOURCE
DATA
CLK
HVOUT (1 of 192)
INPUT BUS (48)
HVGATE
48bit Reg 0/HVOUT
48bit Reg 1/HVOUT
48bit Reg 2/HVOUT
48bit Reg 3/HVOUT
INPUT PROTECT
/BUFFERS
CCKX4
512

Figure 6

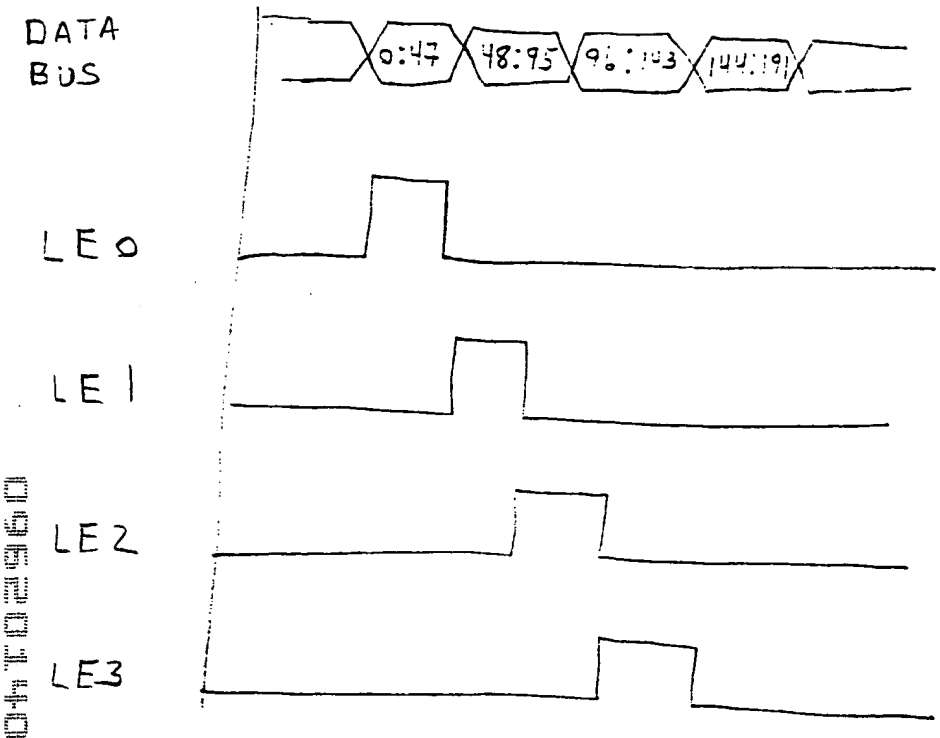
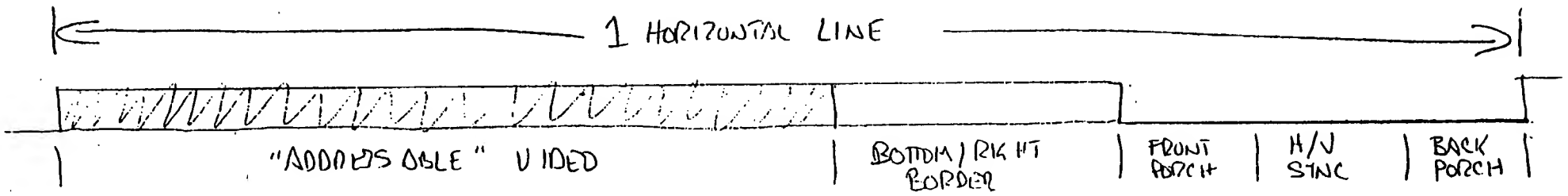


Figure 7

VIDEO TIMING (BASED ON VESA 1021 × 768 @ 60 Hz STANDARD)



DIGITAL TIMING

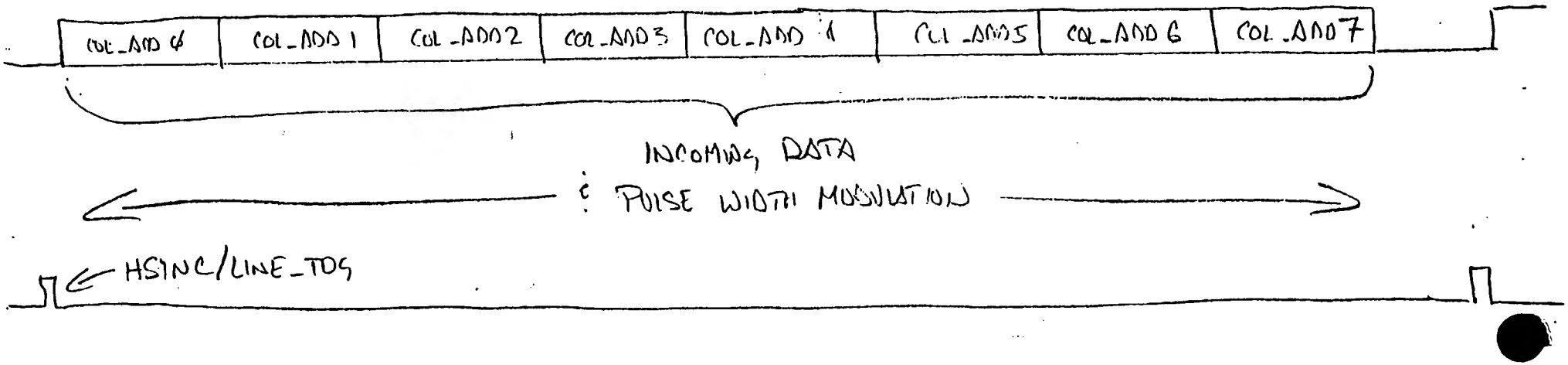


Figure 8

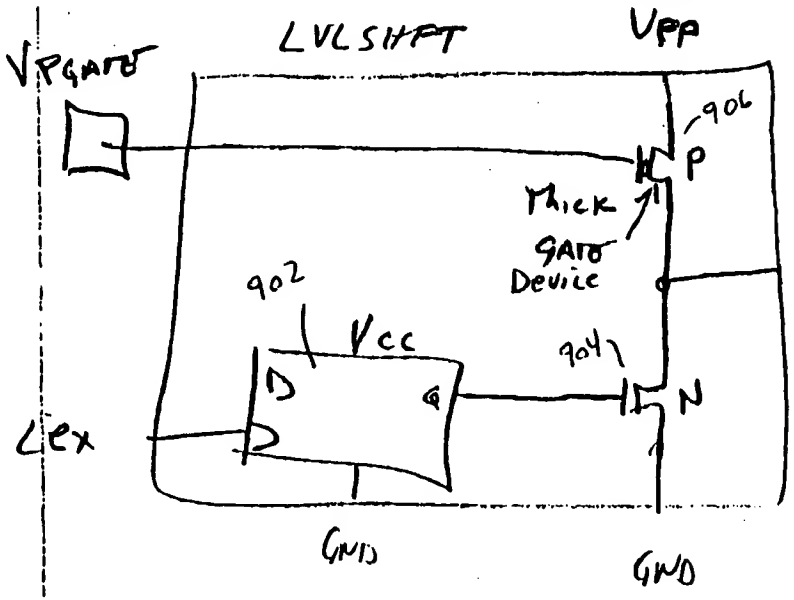


Figure 9A

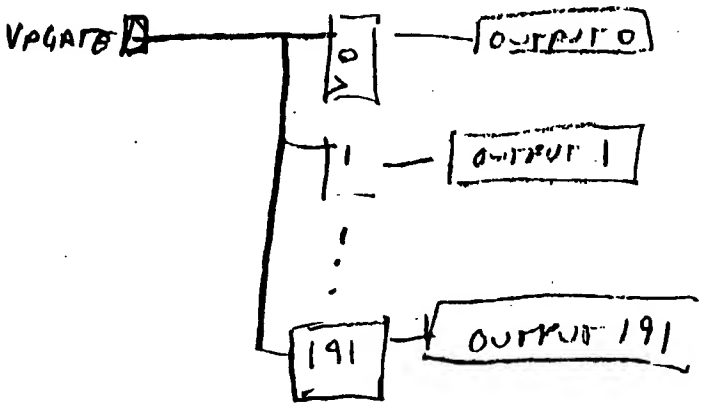


Figure 9B

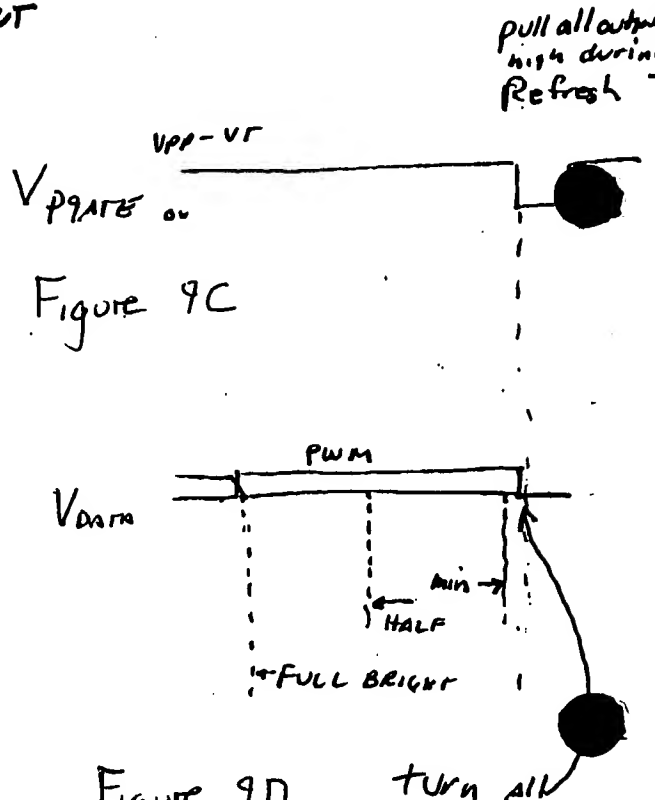


Figure 9C

Figure 9D

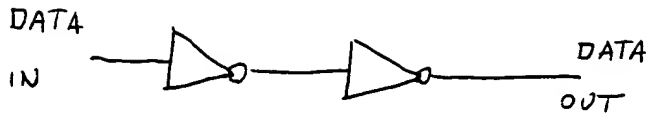


Figure 10A

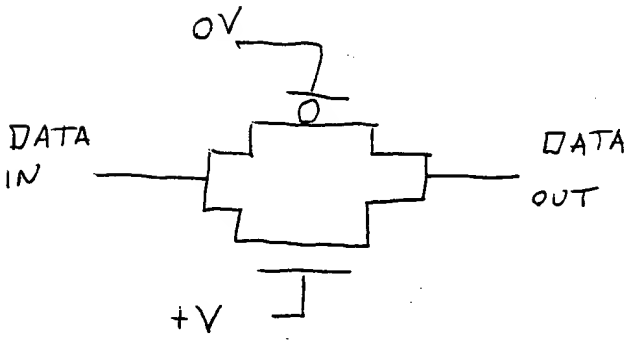


Figure 10B

$t_{VIDEO\ DATA} <= \#Rows \cdot \#Refres[illegible] = \frac{1}{768 \cdot 72} < 18\mu s$

use this full 18 μs - standard VALID VIDEO will be about 80% or 14.5 μs

Fig. 11A HS

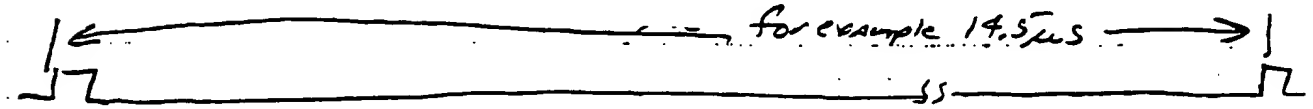


Fig. 11B VIDEO

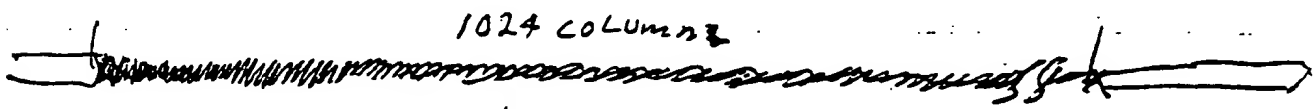


Fig. 11C Pixel CLOCK

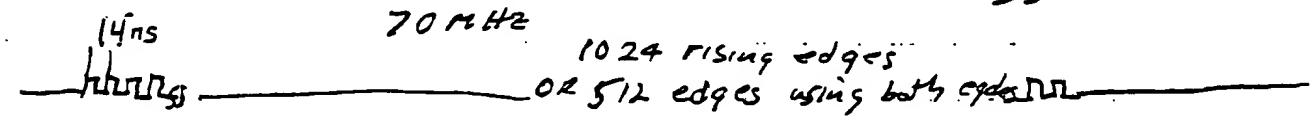


Fig. 12A HS

Fig. 12B VIDEO

Fig. 12C pixel clk

VIDEO to PWM CLK

PW

Fig. 12D

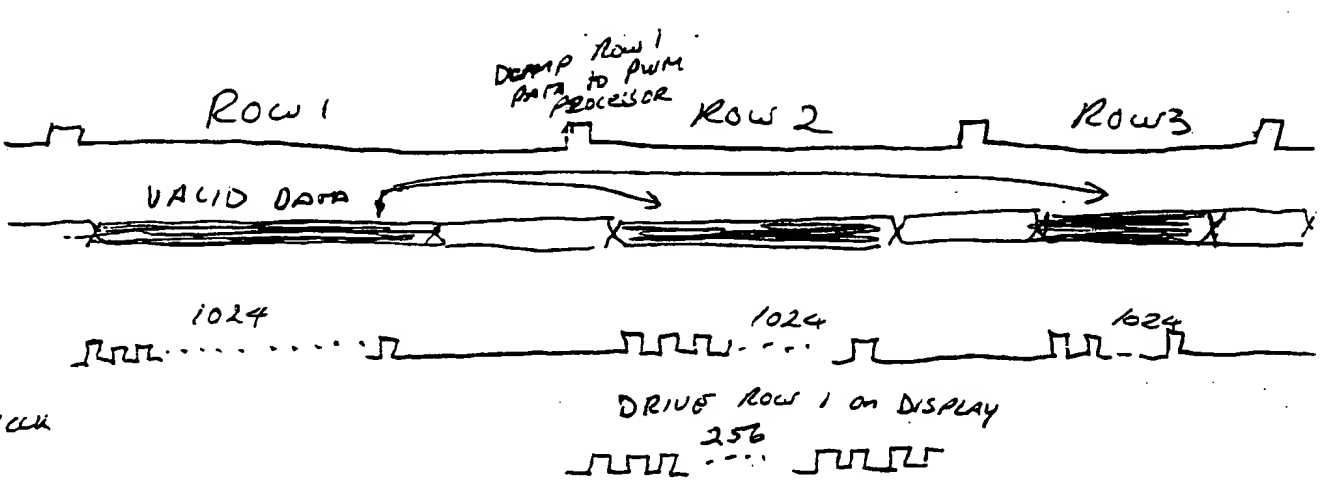


Fig. 13